JPC connectivity

JPC Connectivity Inc.
PRODUCT SPECIFICATION

TITLE	DOC No. RFD-20260706100-003	
800G OSFP-IHS 2XSR4 (SR8) 100m Transceiver	REVISION : 01	AUTHORIZED BY : Hawk Rong
	DATE : 2026/07/06	CLASSIFICATION : Optical Transceiver

1. Product Features

- 53.125GBd PAM4 ×8 channel Optical interface
- 53.125GBd PAM4 ×8 channel Electrical interface
- Up to 100m transmission distance on OM4/OM5 MMF
- 850nm VCSEL and PIN receiver
- OSFP MSA Type2 package with 2*MPO-12 APC
- Very low EMI and excellent ESD protection
- +3.3V power supply
- Power consumption less than 15.5W
- Operating case temperature: 15~70°C
- IIC rate up to 1MHz

2. Product Applications

- 800G Ethernet
- 2x400G InfiniBand

3. Product Compliance

- Compliant with OSFP MSA
- Compliant with IEEE 802.3db
- Compliant with IEEE 802.3ck
- Compliant with CMIS Rev4.0
- Compliant with OIF-CEI-5.0
- Compliant with RoHS 2.0

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4. Product Description

This Transceiver is acost-effective module with high performance, which is optimized for data center, supporting data-rate of 8 × 53.125GBd PAM4. Its transmission distance is up to 100m on OM4/OM5 MMF. The module mainly consists of two parts: thetransmitter part and the receiver part. The transmitter part consists of 850nm VCSEL array and driver. The receiver part consists of trans-impedance amplifier (TIA) and PIN photo diode array. The high-speed electrical interface is based on low-voltage logic, with nominal 100-ohm differential impedance, AC coupled in the module. Users can access a series of registers in transceiver to access monitoring and configuration data through two wire serial interfaces. This interface uses a single address, A0h, with a memory map divided into a lower and upper area. Basic digital diagnostic data is held in the lower area while specific data is held in a series of tables in the high memory area.

4.1 Product Name And Series Number(S)

800G OSFP IHS 2xSR4 100m Transceiver

JPC P/N	Laser (nm)	Distance	Fiber Type	Connector	Temp
P69**LKRCAS1-1	850	100m	MMF	2* MPO12/APC	C

Note-1： ** **Indicates the customer code.**

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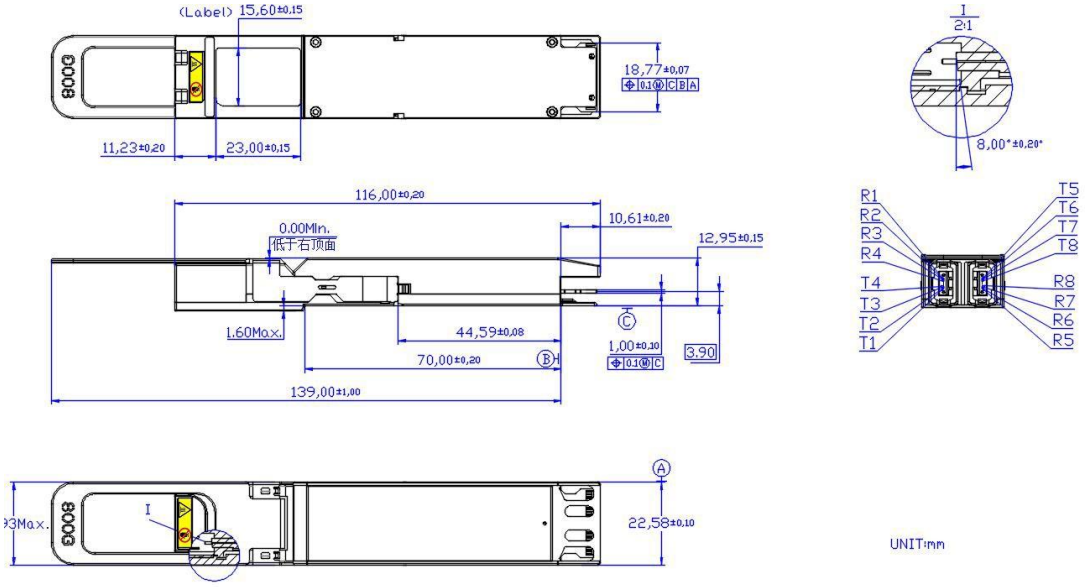
4.2 Dimensions,Materials,Platings And Marking



Notes:

[1] Flatness: 0.12mm or better for the thermally conductive area.

[2] Roughness: 1.6um or better for the thermally conductive area.

5. Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	TSTG	-40		85	ºC	
Operating Relative Humidity		5		85	%	
Supply Voltage	VCC	-0.5		3.6	V	
Optical Input Power	PIN	5			dBm	

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6. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Case temperature	Tcase	15		70	℃	
Supply Voltage	VCC	3.135	3.3	3.465	V	
Supply Current	ICC			4945	mA	
Module Power Dissipation	P			15.5	W	

7. Transmitter Operating Characteristic-Optical，Electrical

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Data Rate per channel（PAM4）	DR		53.125		GBd	
Frequency tracking	Ft	-100		100	Ppm	
Center Wavelength	λ_C	842		868	nm	
RMS Spectral Width				0.65	nm	Note1
Laser Off Power	Poff			-30	dBm	
Average Optical Power	Pavg	-4.6		4	dBm	
Extinction Ratio	ER	2.5			dB	
Transmitter and dispersion eye closure	TDECQ			4.4	dB	
Outer Optical Modulation Amplitude	OMAouter	-2.6		3.5		Note2
Encircled flux, each lane	dB	≥ 86% @ 19 μm, ≤ 30% @ 4.5 μm				Note3
Optical Return Loss Tolerance				14	dB	

Notes:

[1] RMS spectral width is the standard deviation of the spectrum.

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[2] if max(TECQ,TDECQ)≤1.8dB, the OMA (min)=-2.6 ； if 1.8 ＜max(TECQ,TDECQ)≤4.4dB, the OMA (min)= -4.4+max(TECQ,TDECQ)；

[3] If measured into type A1a.2, type A1a.3 or type A1a.4, 50μm fiber, in accordance with IEC 61280-1-4.

8. Receiver Operating Characteristic-Optical，Electrical

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data Rate per channel（PAM4）	DR		53.125		GBd	
Frequency tracking	Ft	-100		100	ppm	
Center Wavelength	λr	842		870	nm	
Average receive power		-6.4		4	dBm	Note1
Receiver Reflectance				-15	dB	
Receiver sensitivity(OMAouter)				Max(-4.6,-6.4+TECQ)		Note2
Differential Data Output Voltage Peak to Peak Swing，Short mode	Vopp			600	mV	
Differential Data Output Voltage Peak to Peak Swing，Long mode	Vopp			845	mV	
Eye height	EH	15			mV	
Vertical eye closure	Vec			12	dB	
Differential output Impedance	Zos	90	100	110	ohm	
Common-Mode to differential-mode return loss	RLdc	Note2				
Transition Time, 20 to 80%	Tr, Tf	8.5			ps	

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Notes:

[1]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

[2] If TECQ≤1.8dB, the OMA (min)=-4.6;Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ up to 4.4 dB

$$RLdc(f) \geq \begin{cases} 25 - 22(f/53.125) & 0.05 \leq f \leq 26.56 \\ 19 - 10(f/53.125) & 26.56 < f \leq 50 \end{cases}$$

9. Digital Diagnostic Functions

Parameter	Symbol	Min.	Max.	Unit	Note
Temperature monitor absolute error	DMI_Temp	-3	3	℃	Over operating temp
Laser power monitor absolute error	DMI_TX	-3	3	dB	
RX power monitor absolute error	DMI_RX	-3	3	dB	
Supply voltage monitor absolute error	DMI_VCC	-3	3	%	
Bias current monitor absolute error	DMI_Ibias	-10	10	%	

10. Control and Status I/O Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
MgmtInitDuration	Max MgmtInit Duration			2000	ms	Note1
ResetL Assert Time	t_reset_init	10			μs	Note2
IntL Assert Time	ton_IntL			200	ms	Note3
IntL Deassert Time	toff_IntL			500	μs	Note4

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Rx LOS Assert Time	ton_los			100	ms	Note5
Flag Assert Time	ton_flag			200	ms	Note6
Mask Assert Time	ton_mask			100	ms	Note7
Mask Deassert Time	toff_mask			100	ms	Note8

Notes:

[1] Time from power on, hot plug or rising edge of reset until completion of the MgmtInit State.

[2] Minimum pulse time on the ResetL signal to initiate a module reset.

[3] Time from occurrence of condition triggering IntL until Vout:IntL=Vol.

[4]Time from clear on read operation of associated flag until Vout:IntL=Voh.This includes deassert times for Rx LOS, Tx Fault and other flag bits.

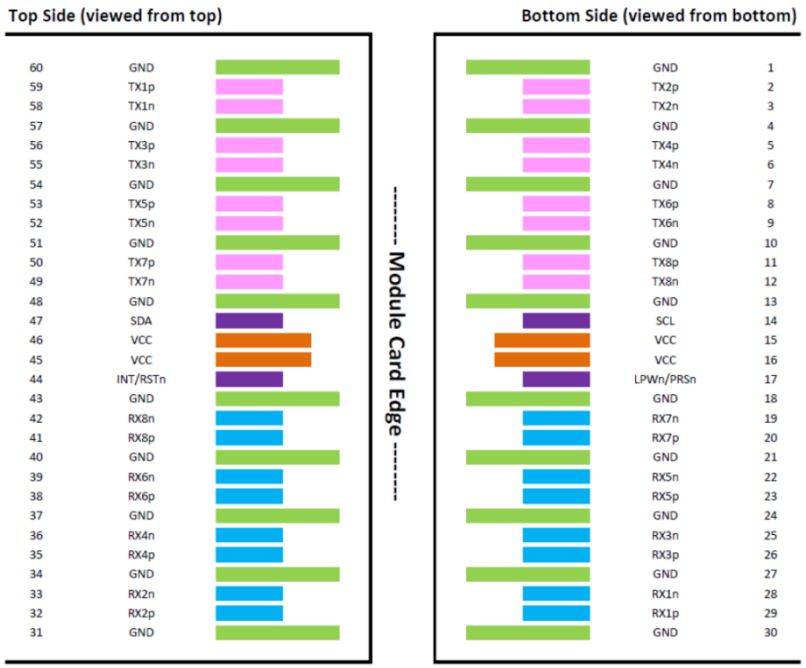
[5] Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.

[6] Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.

[7] Time from mask bit set (value=1b) until associated IntL assertion is inhibited.

[8] Time from mask bit cleared (value=0b) until associated IntL operation resumes.

11. Pin-out Definition



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Pin Assignment

Pad	Logic	Symbol	Name/Description	Plug Sequence	Note
1		GND	Ground	1	
2	CML-I	TX2p	Transmitter Non-Inverted Data Output	3	
3	CML-I	TX2n	Transmitter Inverted Data Output	3	
4		GND	Ground	1	
5	CML-I	TX4p	Transmitter Non-Inverted Data Output	3	
6	CML-I	TX4n	Transmitter Inverted Data Output	3	
7		GND	Ground	1	
8	CML-I	TX6p	Transmitter Non-Inverted Data Output	3	
9	CML-I	TX6n	Transmitter Inverted Data Output	3	
10		GND	Ground	1	
11	CML-I	TX8p	Transmitter Non-Inverted Data Output	3	
12	CML-I	TX8n	Transmitter Inverted Data Output	3	
13		GND	Ground	1	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	3	
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	3	
18		GND	Ground	1	
19	CML-O	RX7n	Receiver Inverted Data Input	3	
20	CML-O	RX7p	Receiver Non-Inverted Data Input	3	
21		GND	Ground	1	
22	CML-O	RX5n	Receiver Inverted Data Input	3	
23	CML-O	RX5p	Receiver Non-Inverted Data Input	3	
24		GND	Ground	1	

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25	CML-O	RX3n	Receiver Inverted Data Input	3	
26	CML-O	RX3p	Receiver Non-Inverted Data Input	3	
27		GND	Ground	1	
28	CML-O	RX1n	Receiver Inverted Data Input	3	
29	CML-O	RX1p	Receiver Non-Inverted Data Input	3	
30		GND	Ground	1	
31		GND	Ground	1	
32	CML-I	RX2p	Receiver Non-Inverted Data Input	3	
33	CML-I	RX2n	Receiver Inverted Data Input	3	
34		GND	Ground	1	
35	CML-I	RX4p	Receiver Non-Inverted Data Input	3	
36	CML-I	RX4n	Receiver Inverted Data Input	3	
37		GND	Ground	1	
38	CML-I	RX6p	Receiver Non-Inverted Data Input	3	
39	CML-I	RX6n	Receiver Inverted Data Input	3	
40		GND	Ground	1	
41	CML-I	RX8p	Receiver Non-Inverted Data Input	3	
42	CML-I	RX8n	Receiver Inverted Data Input	3	
43		GND	Ground	1	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	3	
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	
47	LVCMOS-I/O	SDA	2 wire serial interface data	3	
48		GND	Ground	1	
49	CML-I	TX7n	Transmitter Inverted Data Output	3	
50	CML-I	TX7p	Transmitter Non-Inverted Data Output	3	

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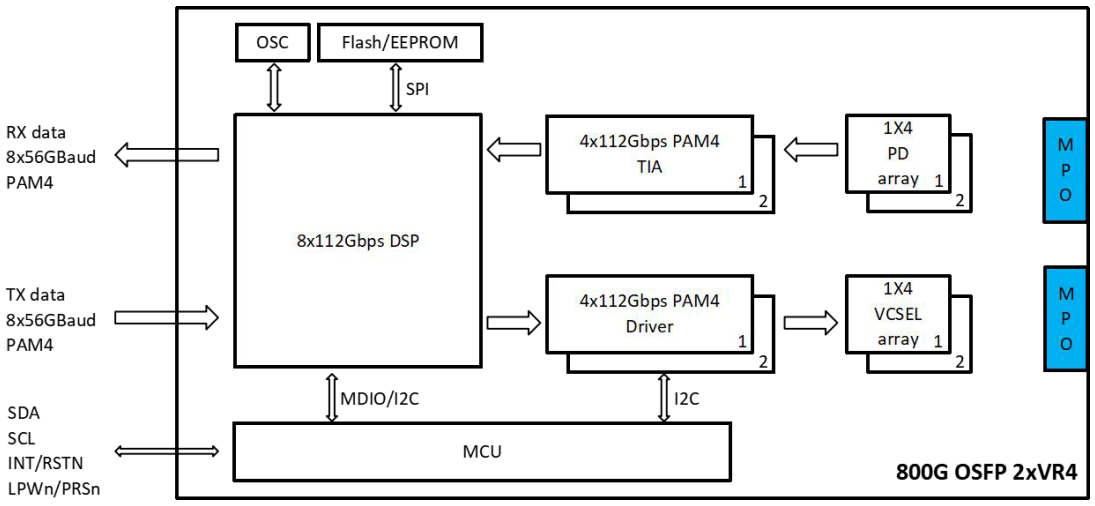
51		GND	Ground	1	
52	CML-I	TX5n	Transmitter Inverted Data Output	3	
53	CML-I	TX5p	Transmitter Non-Inverted Data Output	3	
54		GND	Ground	1	
55	CML-I	TX3n	Transmitter Inverted Data Output	3	
56	CML-I	TX3p	Transmitter Non-Inverted Data Output	3	
57		GND	Ground	1	
58	CML-I	TX1n	Transmitter Inverted Data Output	3	
59	CML-I	TX1p	Transmitter Non-Inverted Data Output	3	
60		GND	Ground	1	

Block Diagram of Transceiver



<Transmitter Section>: The electrical signal is processed by DSP and sent to driver. After receiving the electrical signal from DSP, driver drives VCSEL to convert the electrical signal into optical signal for transmission

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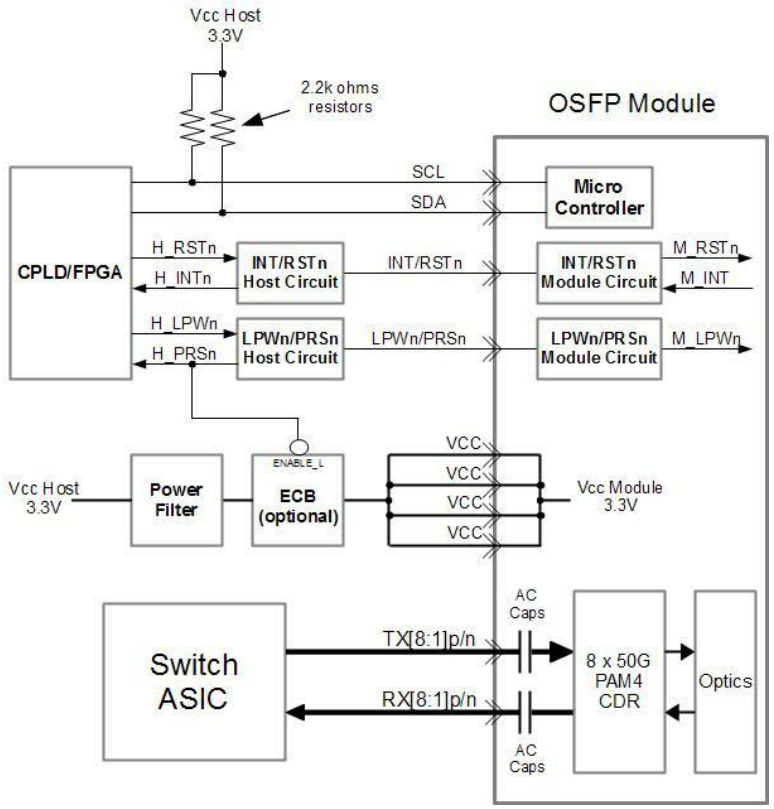
<Receiver Section>: PD converts the received optical signal into electrical signal and transmits it to TIA. TIA amplifies the signal and transmits it to DSP for further processing and sends it to host

Recommended Interface Circuit



12. Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2026/07/06	Hawk Rong	Mike Sun